IN THE CLAIMS:

Please cancel claims 15-18 and 35-57 without prejudice.

Please add the following new claims:

58. In a computer system comprising a master device and at least one memory device, a bus system for transmitting memory requests to the memory device compromising:

a plurality of bus lines for transmission of memory requests;

a packet comprising a memory request for transmission across the bus lines, said packet comprising;

a first word comprising;

start information indicating the start of the packet,

a first portion of lower order memory address bits comprising information to perform page mode memory access, and

a first portion of op code information; and

a second word comprising;

a second and third portion of op code information, wherein an op code for page mode accesses can be detected from the first, second and third portions of op code information, and

a second portion of the lower order memory address bits;

wherein page mode accesses can be performed after transmission of the second word packet.

59. The bus system as set forth in Claims 58 wherein said start information is located at a predetermined location in the first word of the packet, said system further comprising;

means for monitoring the predetermined location in each word during transmission of subsequent words of the packet for information other than the start of the packet; and

means for detecting a collision if information occurs at the predetermined location in subsequent words of the packet, said information occurring due to the start information of a second packet overlapping the first packet.

60. The bus system as set forth in Claim 59, wherein said packet further comprises a code identifying the device transmitting the packet, said means for detecting a collision further comprising means for detecting the code to determine whether the code is valid, an invalid code resulting from a collision of packets.

61. The bus system as set forth in Claim 58, wherein said packet further comprises count information indicating the number of bytes of memory to be transmitted across the bus lines during the memory transaction requested.

62. The bus system as set forth in Claim 61, wherein said data is transmitted in a multiple byte block format, said system further comprising:

means for generating a first mask for the first multiple byte block of the data to be transmitted, said mask indicating the bytes of the multiple byte block which are part of the memory operation requested; and

63. The bus system as set forth in Claim 62, wherein data is transmitted in 4 byte blocks, the first mask is generated from the two least significant bits of the address bits and the second mask is generated from the two least significant bits of the count information.

64. The bus system as set forth in Claim 62, further comprising a first and second lookup table comprising mask patterns, said masks generated by performing a table lookup respectively using the address bits and the count information.

65. The bus system as set forth in Claim 58, further comprising a summing means for summing the two least significant address bits and internal byte count to produce an overflow value and count information, said overflow information indicating that although the size of the data of the memory request is less than the maximum number of bytes allowed in the memory operation, the granularity of the multiple byte block format transmitted across the bus prohibits the transaction and the request should be separated into to separate memory requests.